In the Claims

Kindly amend claims 4, 5, 7 and 8 as shown in the following claim listing:

1. (original) A semiconductor device including a semiconductor body (10) comprising a source region (13) and a drain region (14, 14a) of a first conductivity type, having therebetween a channel-accommodating region (15), the drain region comprising a drain drift region (14) and a drain contact region (14a), with the drain drift region between the channel-accommodating region and the drain contact region, and the drain drift region being doped to a lesser degree than the drain contact region, an insulated gate (11) separated from the channel-accommodating region (15) by a gate insulating layer (17), and a localised region (30,36,50) in the drain drift region (14a) juxtaposed with the channel-accommodating region (15), the localized region (30,36,50) comprising alternating stripes (31,32) of the first conductivity type and a second, opposite conductivity type, which stripes extend laterally alongside the channel-accommodating region (15) and away from the gate (11), the dimensions and doping levels of the stripes being such that the localized region provides a voltage-sustaining space-charge zone when depleted.

2.(original) A device of claim 1, wherein the localised region (30,36,50) adjoins the channel-accommodating region.

3. (original) A device of claim 1, wherein the localised region (36) is laterally spaced from the gate insulating layer.

4.(currently amended) A device of ~~any preceding Claim~~ claim 1, 2 or 3 wherein the average doping level of the localized region (30,36,50) is substantially the same as that of an adjacent portion of the drain drift region.

5.(currently amended) A device of ~~any preceding Claim~~ claim 1, 2 or 3, wherein the gate (11) is provided in a trench (20), the trench extending through the channel-accommodating region (15) into the drain drift region (14a).

6. (original) A device of Claim 5 comprising a plurality of adjacent cells, each including a gate (11) in a trench (20), wherein a deep diffusion region (40) of the second conductivity type is provided between adjacent trenches, the deep diffusion region (40) being doped to a greater extent that the channel-accommodating region (15).

7. (currently amended) A device of Claim 5 ~~or Claim 6~~ wherein the lower boundary (30b) of the localized region (30,36) is above the bottom of the gate trenches.

8. (currently amended) A device of ~~any preceding Claim~~ claim 1, 2 or 3 wherein the channel-accommodating region (15) is a region of an opposite, second conductivity type.

9. (original) A method of manufacturing a semiconductor device including a semiconductor body (10) comprising a source region (13) and a drain region (14,14a) of a first conductivity type, having therebetween a channel-accommodating region (15), the drain region comprising a drain drift region (14a) and a drain contact region (14), with the drain drift region between the channel-accommodating region and the drain contact region, and the drain drift region being doped to a lesser degree that the drain contact region, and an insulated gate (11) separated from the channel-accommodating region (15) by a gate insulating layer (17), the method including the step of:

forming a localised region (30,36,50) in the drain drift region (14a) juxtaposed with the channel-accommodating region (15), the localized region (30,36,50) comprising alternating stripes (31,32) of the first conductivity type and a second, opposite conductivity type, which stripes extend laterally alongside the channel-accommodating region (15) and away from the gate (11).

10. (original) A method of Claim 9 wherein the localised region (30,36,50) forming step comprises implanting a dopant of one of the first and second conductivity types, defining a striped mask (35) over the semiconductor body (10), and implanting a dopant of the other of the first and second conductivity types.